A flexible organic pentacene nonvolatile memory based on high-\(\kappa\) dielectric layers

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(Received 8 September 2008; accepted 20 November 2008; published online 10 December 2008)

We report a pentacene thin film transistor nonvolatile memory fabricated on a flexible polyimide substrate. This device shows a low program/erase voltage of 12 V, a speed of 1/100 ms, an initial memory window of 2.4 V, and a 0.78 V memory window after 48 h. This has been achieved by using a high-\(\kappa\) dielectric as charge trapping, blocking, and tunneling gate insulator layers. © 2008 American Institute of Physics. [DOI: 10.1063/1.3046115]

Organic nonvolatile memory devices have potential applications in flexible display drive logic, radio frequency identification tags, and smart cards.1,2 These nonvolatile memory devices supply an essential function for integrated circuits (ICs) based on organic thin-film transistors (OTFTs). The advantages of using organic memory devices, over their inorganic counterparts, are in their low cost, light weight, simple structure, mechanical flexibility, and low-temperature processing. For system-on-chip application, the nonvolatile memory function is required. The OTFT-based nonvolatile organic memory devices display high drive current, low off-state leakage current, and reasonably fast switching speeds. The memory properties of these OTFT-based devices arise from the electric field modulation in the gate insulator through the spontaneous polarization of ferroelectrics2–4 or because of charge trapping in a chargeable layer.5,6 The charge-trapping type of OTFT memory device employs the well-known device physics of such structures and can build on the manufacturing experience of the Si industry. Digital data can be programed into the device by injecting charges into the gate insulator or erased by removing the stored charges. This charge transfer in the gate dielectric is readable by measuring the threshold voltage \(V_{th}\) of the transistor. This program or erase function can be obtained by having a large electric field across the gate insulator. Previous charge-trapping OTFTs have used a polymer as the trapping layer5 or a floating gate,6 necessitating a high gate voltage \(V_g\) to write the data. Such high voltages are incompatible with low-power IC designs and challenge existing battery technology. A solution to lowering the program and erase voltages is to use a high-\(\kappa\) dielectric. This has been done by incorporating a high-\(\kappa\) dielectric as the gate insulator in the OTFTs, leading to lower voltage operation.7–9

A schematic diagram of the OTFT nonvolatile memory is shown in Fig. 1(a). The OFET memory devices were fabricated on 125 \(\mu m\) thick polyimide (PI) substrates (Kapton HPP-ST, Dupont). Prior to device fabrication, the substrates were cleaned in de-ionized water and annealed in a vacuum of \(3 \times 10^{-6}\) torr at 200 °C to improve the dimension stability. A 100 nm SiO\(_2\) thin film was deposited on the substrate by electron beam evaporation to create a layer with low internal stress. A 50 nm TaN gate electrode was then deposited by reactive sputtering through a shadow mask. This was given a NH\(_3\) plasma treatment to improve the metal-electrode/high-\(\kappa\) interface.9 The 20 nm HfLaO\(_x\), 20 nm HfON, and 6 nm HfO\(_2\) were then deposited by physical vapor deposition and given a 200 °C, 30 min furnace treatment in O\(_2\) to improve the gate oxide quality. This was followed by deposition through a shadow mask of the pentacene active layer (Aldrich Chemical Co.) that was 70 nm thick. (The deposition conditions were as follows: a deposition rate of 0.5 Å/s at a pressure of \(3 \times 10^{-6}\) torr, with the substrate being held at 70 °C.) Finally, 50 nm of gold was deposited at rate of

![Schematic cross-sectional diagram of the flexible pentacene OTFT memory devices.](image)

**FIG. 1.** (a) Schematic cross-sectional diagram of the flexible pentacene OTFT memory devices. (b) Transfer characteristics of pentacene OTFT memory devices.

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1 Å/s for the source/drain electrodes. The channel width and channel length were 1500 and 150 μm, respectively. All electrical characteristics were made using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter in the dark and an air ambient.

The transfer characteristics for OTFT memory device are displayed in Fig. 1(b). From the transfer characteristics, the mobility $V_{th}$, subthreshold swing (SS), and on/off current ratio ($I_{on}/I_{off}$) were 0.1 cm²/V s, −1.4 V, 160 mV/decade, and $1 \times 10^{4}$ in the saturation region at a drain voltage ($V_d$) of −3 V. The low $V_{th}$ and good SS are due to the use of a high-$\kappa$ material as gate dielectric.7–9

The energy band diagram of our OTFT memory device is shown in Fig. 2.10–12 The HfLaO gate dielectric has a high dielectric constant, large bandgap, and high electron injection barrier with respect to the TaN gate electrode during the erase process.9 A proper thickness of HfLaO blocking layer is important to reduce gate leakage current. The higher gate leakage current will degrade the mobility, SS, and retention time of OTFT memory devices. The small band-gap HfON12–14 with its deep trapping energy was chosen as the charge-trapping layer to achieve good charge trapping characteristics. The thin HfO₂ dielectric serves as a charge-tunneling layer and charge-blocking layer. The gold electrode forms an Ohmic-like contact for the injection of holes. When a proper gate bias is applied, the charges in the pentacene active layer tunnel through the HfO₂ are trapped in the HfON layer. When a proper gate bias is applied, the charges in the pentacene active layer tunnel through the HfO₂ are trapped in the HfON layer.

In Fig. 3, we show the shift in the transfer characteristics at $V_d=−1$ V, under a gate bias of −12 V at 1 ms for the program, and +12 V at 100 ms for the erase process. The drain current-gate voltage ($I_d-V_g$) curve shifted in a negative direction when a $V_g$ of −12 V was applied for 1 ms, and in a positive direction after application of a reverse $V_g$ of 12 V for 100 ms. Thus the $V_{th}$ value can be shifted reversibly by applying an appropriate gate bias. A 2.6 V $V_{th}$ shift was shown after a −12 V program voltage pulse was applied for 1 ms. This could be erased with a large 2.5 V $V_{th}$ shift after a +12 V voltage pulse for 100 ms. Since a negative voltage was applied across the HfLaO/HfON/HfO₂ gate dielectric stack during the programing process, hole accumulation occurred at the dielectric/pentacene interface. The increase in the $V_{th}$ shift with the increase in negative $V_g$ indicates that the accumulated holes were injected over the HfO₂ gate dielectric and stored in the lower energy HfON dielectric. The erase was performed by applying a positive $V_g$ to the TaN gate electrode, where the applied electric field over the HfO₂ gate dielectric is shown after a −12 V program voltage pulse was applied for 1 ms. This could be erased with a large 2.5 V $V_{th}$ shift after a +12 V voltage pulse for 100 ms. Thus the $V_{th}$ value can be shifted reversibly by applying an appropriate gate bias. A 2.6 V $V_{th}$ shift was shown after a −12 V program voltage pulse was applied for 1 ms. This could be erased with a large 2.5 V $V_{th}$ shift after a +12 V voltage pulse for 100 ms. Since a negative voltage was applied across the HfLaO/HfON/HfO₂ gate dielectric stack during the programing process, hole accumulation occurred at the dielectric/pentacene interface. The increase in the $V_{th}$ shift with the increase in negative $V_g$ indicates that the accumulated holes were injected over the HfO₂ gate dielectric and stored in the lower energy HfON dielectric. The erase was performed by applying a positive $V_g$ to the TaN gate electrode, where the applied electric field over the

HfLaO/HfON/HfO₂ gate dielectric stack causes hole depletion in the pentacene. The stored holes in the HfON may tunnel out over the HfO₂ gate dielectric into the pentacene; alternatively, the minority carriers (electrons) generated in the depletion region of the pentacene can also tunnel through the HfO₂ and into the HfON, all of which give rise to the erase function. Similar mechanisms have also been suggested by us to explain the program and erase functions in Si-based nonvolatile memory.12–16 The shift in capacitance-voltage characteristics for a TaN–HfLaO–HfON–HfO₂-pentacene-Au metal-insulator-semiconductor capacitor is shown in Fig. 3(b).

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12 V at 100 ms for the erase function. In Fig. 4, we show the retention data. The $V_{th}$ was extracted in the linear region of the $I_d$-$V_g$ characteristics at $V_d = -1$ V. The initial memory window was 2.4 V, which decreased to 0.78 V after 48 h. The significant charge loss of $\sim 50\%$ at $10^3$ s is possibly related to the increase in the leakage current due to the surface roughness of the PI substrates, as well as defects in the low-temperature-formed HfO$_2$. Atomic force microscopy showed that the rms surface-roughness was approximately 5 nm. Improvements in the leakage current can be expected from smoother substrates and replacing the HfO$_2$ with a higher-quality gate dielectric.

In summary, we have fabricated organic pentacene non-volatile OTFT memory devices on flexible PI substrates. These devices used a high-$\kappa$ HfON dielectric as the charge trapping layer, HfLaO as blocking layers and HfO$_2$ as the tunneling layer. We found program/erase voltages of $-12/-12$ V, at a speed of 1/100 ms along with an initial memory window of 2.4 V.

This work has been supported in part by NSC Contract No. 97-2120-M-009-008.